

Transient and Stability Analysis of Voltage Switch Charge Pump PLL

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ABSTRACT

Phase-Locked Loops (PLLs) are widely used in modern communication, sensing and digital systems for frequency synthesis, clock generation, and synchronization. Understanding their transient behavior and stability is essential for achieving fast, accurate, and reliable operation. In This paper presents an analytical study of transient dynamics and stability of second- and third-order Voltage Switch Charge Pump Phase-Locked Loop (VSCP-PLL) architectures for high-speed communication and sensing. A unified framework combines small-signal linearization, nonlinear modeling, and state-space formulation for both loop orders. For the second-order loop, closed-form natural frequency and damping ratio expressions enable direct prediction of overshoot, settling time, and lock behavior. The third-order model captures added pole-zero interactions and higher-order coupling, explaining phase accumulation and stability degradation. Key parameters charge-pump current, loop-filter pole-zero placement, VCO gain, and divider ratio are examined versus transient response and phase/frequency error. Stability margins are quantified via Bode analysis, highlighting phase/gain-margin reductions from the extra pole. Controllability and observability are verified to support digital-assist and adaptive control. Simulations and event-driven transients validate derived stability and robust design region. Results show third-order filtering improves spur/ripple suppression but increases mismatch sensitivity and lock-time variability. For this study MATLAB R2020a is used for simulation alongside Simulink.

1. Introduction

Phase-Locked Loops (PLLs) are among the most important subsystems in modern mixed-signal and RF integrated circuits, providing frequency synthesis, clock distribution, carrier recovery, and synchronization across a wide range of electronic platforms. With the rise of new high-data-rate communication systems, millimeter-wave transceivers, edge computing devices, and autonomous electronic platforms, Phase-Locked Loop architectures must operate under increasingly severe performance constraints. These include low lock-in time, minimal overshoot, low phase noise, high jitter suppression, and high stability margins under Process-Voltage-Temperature (PVT) variations. Simultaneous fulfillment of these objectives is related to a nontrivial challenge in control and circuit design [1–3]. Among the Phase-Locked Loop implementations, charge pump-based architectures are predominant because they are compatible with the fabrication of circuits in the medium-tension based on CMOS processes, are scalable, and have excellent phase noise performance. In particular, an interesting alternative

to traditional current-steering charge pump designs is the Voltage Switch Charge Pump Phase-Locked Loop (VSCP-PLL). By applying the voltage-mode switching characteristics, the VSCP structures are applied to reduce dead zone effects as well as obtain higher linearity in phase detection and low current mismatch sensitivity. However, these structural benefits come with complex nonlinear switching dynamics, which have a great impact on the transient behavior and stability margins [4, 5]. Fig. 1 illustrates the general VSCP-PLL architecture, including the phase-frequency detector, charge-pump switching network, passive loop filter, voltage-controlled oscillator, and divider-based feedback path.

The dynamic properties of a PLL are almost completely determined by the loop and filter topology order. Second-order PLL's themselves are widely used as a result of their analytical simplicity as well as predictable behavior. Their transient response can be approximated by resorting to the classical second-order control theory with its natural frequency and damping ratio parameters. This representation allows direct control over overshoot,

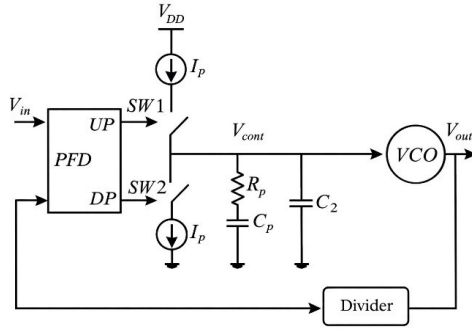


Fig. 1. VSCP-PLL Architecture.

time to settle, and locked-in dynamics. However, in order to realize high-frequency noise attenuation and reference spur suppression functions for high-speed communication systems, the transient performance of second-order loops may be limited. To overcome these disadvantages, third-order loop filters are often added. The addition of the extra pole provides better filtering of high frequencies and spur rejection. However, the inherent gain in system dimensionality and additional pole-zero interactions for the system due to loop-loop interaction when increasing the loop order decrease the phase margin robustness, unless tuned correctly. The resultant higher-order dynamics may lead to oscillatory behavior, increased settling time, and increased sensitivity to variation of charge pump current and VCO gain mismatch [6–8]. Despite serious past efforts made in the issue of PLL stability analysis, most of the studies have considered the second and third-order configurations separately. Furthermore, frequency domain stability characterization is often decoupled from time-domain transient evaluation to limit design insight [9, 10]. The impact of important design parameters such as the charge pump current magnitude, loop filter pole and zero placement, VCO gain sensitivity, and divider ratio are systematically quantified with respect to lock-in time as well as settling time, overshoot, and phase/frequency error evolution. Furthermore, classical Bode-plot methods are coupled with root-locus interpretation to analyze phase and gain margins explicitly. Controllability and observability conditions are proven formally in order to allow digital-assist and adaptive control extensions. Comparative results indicate fundamental trade-offs between second and third-order configurations that offer quantitative design constraints for robust operation.

2. VSCP-PLL Architecture and Linear Model

The Voltage Switch Charge Pump Phase-Locked Loop (VSCP-PLL) architecture shown in Fig. 1 has a fundamental difference from the conventional current-steering charge pump PLL in the way the charge pump gain is determined. In conventional configurations, fixed bias currents are used to set the magnitude of pump current, so that the charge pump gain is constant under steady-state conditions. In contrast, the VSCP-PLL employs voltage-controlled switching of the pump transistors, such that the loop filter control voltage V_{ctrl} directly influences the effective charge pump current [11–15]. Consequently, the charge pump gain becomes state-

dependent and may be expressed as $K_{CP}(V_{ctrl})$. The resulting open-loop transfer function is given by

$$G(s) = \frac{K_{CP}(V_{ctrl}) K_{VCO} F(s)}{Ns} \quad (1)$$

Fig. 2 shows the CP-PLL Architecture. The figure shows how the reference input is compared with the divided output, while the switched charge-pump and loop filter generate the control voltage that tunes the VCO to achieve phase and frequency locking.

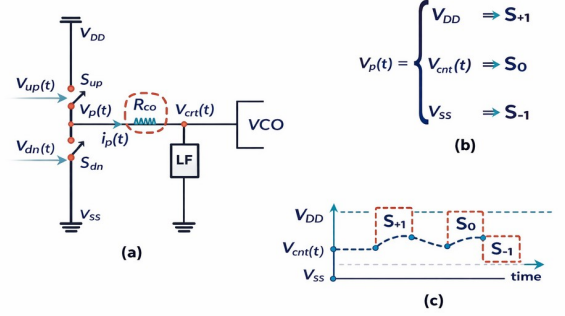


Fig. 2. CP-PLL Architecture

Where K_{VCO} denotes the voltage-controlled oscillator gain in rad/s/V, N is the divider ratio, $F(s)$ represents the loop filter transfer function, and the term s^{-1} arises from the inherent integration property of the VCO [16, 17]. The presence of this integrator guarantees the loop to have a zero steady-state phase error for constant frequency offsets, constituting the loop a type-II PLL. Table 1 shows the Simulation Parameters.

Table 1

Simulation Parameters

Parameter	Second Order	Third Order
f_{ref}	1 MHz	1 MHz
I_{cp}	50 μ A	50 μ A
R_0	60, 120, 150 k Ω	
R_1	20 k Ω	
V_{dd}	2.5 V	
K_v	31.68 MHz/V, 48 MHz/V, 96 MHz/V	
N	96	
C_1	350 pF	
C_2		35 pF

3. Controllability and Observability Analysis

Controllability and observability are basic structural parameters to determine whether or not (or in which form) a dynamic system is amenable to state-feedback or observer-based control augmentation. In Voltage Switch Charge Pump Phase-Locked Loops (or VSCP-PLLs), these properties are especially important because of the voltage-dependent gain characteristic of the charge pump as well as the increased order pole interactions in advanced loop filter configurations [18]. Even in cases where transient performance may seem acceptable, a lack of structural controllability or poor numerical conditioning in signal-conditioning systems can

render digital assist stabilization strategies ineffective or unstable.

The Controllability Gramian matrix is used in control systems to determine how easily the states of a dynamic system can be controlled by its inputs. It is particularly useful for continuous-time linear systems.

For a linear time-invariant state-space model

$$\dot{x}(t) = Ax(t) + Bu(t) \quad (2)$$

$$y(t) = Cx(t) + Du(t) \quad (3)$$

The system is structurally controllable if the controllability matrix has full rank, thus proving that it is theoretically possible to have control over all states. However, meeting the rank condition is only a necessary condition of theoretical feasibility [19]. In actual implementations, the numerical conditioning of the controllability Gramian should also be assessed. For the second-order VSCP-PLL model, the dynamic behavior of the loop can be conveniently represented in state-space form by defining the state vector as

$$x(t) = \begin{bmatrix} \phi_e(t) \\ V_{C1}(t) \end{bmatrix} \quad (4)$$

where $\phi_e(t)$ denotes the instantaneous phase error between the reference input phase and the feedback phase generated by the VCO, and $V_{C1}(t)$ represents the voltage across the primary loop filter capacitor C_1 . where $u(t)$ represents the reference phase input and $y(t)$ corresponds to the VCO output phase. The system matrices are given by

$$A = \begin{bmatrix} 0 & 1 \\ -\omega_n^2 & -2\zeta\omega_n \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \omega_n^2 \end{bmatrix}, \quad (5)$$

$$C = \begin{bmatrix} 1 & 0 \end{bmatrix}, \quad D = 0$$

where ω_n denotes the natural frequency of the PLL and ζ represents the damping ratio. This canonical second-order form clearly highlights the oscillatory nature of the loop and directly relates the PLL parameters to classical control system characteristics such as bandwidth, damping, and transient settling time [19].

3.1 Second Order VSCP-PLL

3.1.1 Controllability

The controllability of the proposed second-order system was evaluated using the controllability matrix defined as

$$C = \begin{bmatrix} B & AB \end{bmatrix} \quad (6)$$

For a second-order system, the system is considered completely controllable if the rank of the controllability matrix equals the system order ($n=2$). Using the system parameters, the obtained controllability matrix is

$$A = \begin{bmatrix} 0 & 1 \\ 1 & -16693 \end{bmatrix} \quad (7)$$

The rank of this matrix is equal to 2, which matches the system order. Therefore, the proposed second-order

system is completely controllable, indicating that all state variables can be influenced by the input signal.

3.1.2 Observability

The observability of the proposed second-order system was analyzed using the observability matrix defined as

$$O = \begin{bmatrix} C \\ CA \end{bmatrix} \quad (8)$$

For a second-order system, the system is considered completely observable if the rank of the observability matrix equals the system order ($n=2$). Using the system parameters, the obtained observability matrix is

$$A = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (9)$$

The rank of this matrix is equal to 2, which is the same as the system order. Therefore, the proposed second-order system is fully observable, indicating that all internal state variables can be reconstructed from the system output.

3.2 Third Order VSCP-PLL

3.2.1 Controllability

For the third-order VSCP-PLL model, the state vector is extended to incorporate the additional energy storage element introduced by the second loop filter capacitor C_2 . The augmented state vector is defined as

$$x(t) = \begin{bmatrix} V_{C1}(t) \\ V_{C2}(t) \\ \phi_{VCO}(t) \end{bmatrix} \quad (10)$$

where $V_{C1}(t)$ and $V_{C2}(t)$ represent the voltages across capacitors C_1 and C_2 , respectively, and $\phi_{VCO}(t)$ denotes the VCO output phase. The inclusion of C_2 introduces an additional pole into the loop transfer function, thereby increasing the system order and modifying the phase margin and stability characteristics [20]. Following linearization of the nonlinear VSCP gain mechanism and transformation of the loop equations into state-space form. Where the system matrix A , computed numerically using the parameter values provided in Table 1, is expressed as

$$A = \begin{bmatrix} \frac{-1}{R_0C_1} & \frac{1}{R_0C_1} & 0 \\ \frac{1}{R_0C_2} & -\left(\frac{1}{R_0C_2} + \frac{1}{R_2C_2}\right) & 0 \\ K_{VCO} & 0 & 0 \end{bmatrix} \quad (11)$$

Substituting the numerical parameter values yields.

$$A = \begin{bmatrix} -2381 & 2381 & 0 \\ 23810 & -1.4524 \times 10^6 & 0 \\ 0 & 4.8e+07 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 7.1429 \\ 0 \\ 0 \end{bmatrix} \quad (12)$$

$$C = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}$$

$$D = \begin{bmatrix} 0 \end{bmatrix}$$

The controllability of the proposed third-order system was evaluated using the controllability matrix defined as $C = [B \ AB \ A^2B]$. For a third-order system, the system is considered completely controllable if the rank of the controllability matrix equals the system order ($n=3$). Using the system parameters, the obtained controllability matrix is

$$P = \begin{bmatrix} 7.1429e4 & -1.7007e8 & 4.4542e12 \\ 0 & 1.7007e9 & -2.4741e15 \\ 0 & 0 & 8.1633e16 \end{bmatrix} \quad (13)$$

The rank of this matrix is equal to 3, which is the same as the system order. Therefore, the proposed system is completely controllable, indicating that all state variables can be influenced by the input signal.

3.2.2 Observability

The observability of the proposed third-order system was analyzed using the observability matrix defined as

$$O = \begin{bmatrix} C \\ CA \\ CA^2 \end{bmatrix} \quad (14)$$

For a third-order system, the system is considered completely observable if the rank of the observability matrix equals the system order ($n=3$). Using the derived state-space matrices, the obtained observability matrix is

$$O = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 4.8e+07 & 0 \\ 1.1429e+12 & -6.9714e+13 & 0 \end{bmatrix} \quad (15)$$

The rank of this matrix is equal to 3, which is the same as the system order. Therefore, the proposed system is fully observable.

4. Results and Discussion

4.1 Dynamic Response and Stability of Second- and Third-Order VSCP-PLL

The dynamic response and stability robustness properties of Voltage Switch Charge Pump Phase-Locked Loops (VSCP-PLL) are inherently governed by the structural properties of the feedback loop, namely the

loop order, pole-zero properties, and overall gain allocation of the charge pump loop filter as well as the voltage-controlled oscillator stages.

4.2 Transient Dynamics and Parametric Sensitivity

The transient response of a Phase-Locked Loop is basically dominated by the interaction of natural frequency, damping ratio, loop bandwidth, and high-frequency pole-zero distribution. In more practical implementations of VSCP-PLLs, these parameters are not independent of each other; instead, they are a combination of charge pump gain, loop filter impedance, and VCO sensitivity. The acquisition process is a dynamic process, which is thus the visible result of inner pole migration and phase accumulation over the feedback loop process [21, 22]. The effect of the transient waveform envelope of the primary loop filter capacitor C1 is shown in Fig. 3 for different values of the loop filter capacitor C1.

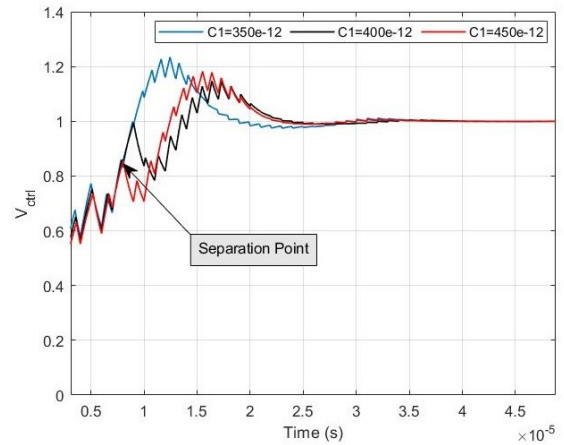


Fig. 3. Transient response of Third-order VSCP-PLL under C1 variation.

The separation point (Fig. 3) is a very important phenomenon in the dynamics of the second-order VSCP-PLL. It represents a major transition point in which the system response is extremely sensitive to small changes in C1 capacitance. Before this point, the transient responses of the PLL are similar; however, past this point, even small variations in capacitance introduce fairly large divergence in the behavior of the system. This is an important factor to understand, as the stochastic nature of the system means that small changes in capacitance have a drastic effect on the phase-locking, stability, and overall dynamic response of the PLL. The separation point assists in determining the boundaries in which the system performance shows more dependence on C1 and, therefore, requires precise adjustment to obtain optimal operating conditions [23]. However, this improvement in stability robustness comes at the cost of some decrease in the bandwidth of the loop, directly affecting the increase in the time of settlement [24]. In contrast, some additional dynamic coupling is observed in the case of the third-order VSCP-PLL since some additional filter capacitor is used [25]. This extra element for energy storage creates a three-pole system which interacts with a dominant pole pair, producing more complicated forms of transient behavior. The system is

now no longer in control of a single dominant oscillatory mode, but a number of oscillating, interacting dynamic states.

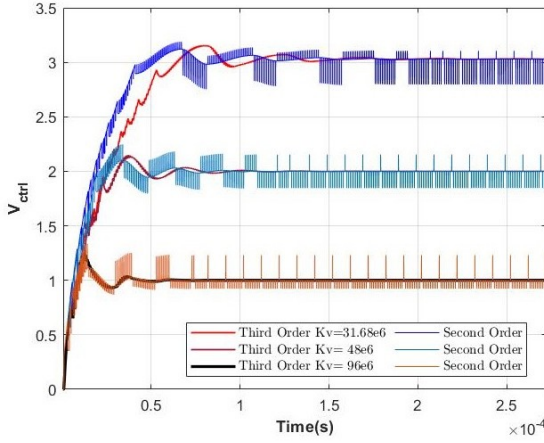


Fig. 4. Comparative analysis of K_v variation on second and third-order VSCP-PLL transient behavior.

Fig. 4 compares the transient responses of second and third-order VSCP-PLLs with different values of K_v (31.68 MHz, 48 MHz, and 96 MHz). The third-order system has better stability and less overshoot, especially when K_v values are higher, while the second-order system has faster convergence but higher overshoot. The sensitivity of the Transient response to variation of R_0 (Third order) is shown in Fig. 5.

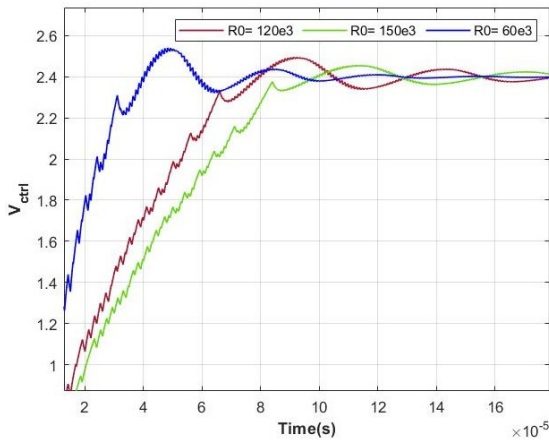


Fig. 5. Transient response sensitivity to R_0 variation (Third order).

Reducing R_0 (zero frequency up, effective loop gain (+), phase margin (-)). As R_0 decreases, overshoot will increase, and oscillation tails will be more pronounced. This confirms the statement that zero placement is the dominant damping tuning mechanism of higher-order VSCP-PLLs. Unlike capacitor scaling, which alters the natural frequency, zero placement has a direct effect on phase margin around crossover. The effect of secondary capacitor C_2 is shown in Fig. 6. This component adds an extra pole that manipulates high-frequency phase response and ripple characteristics.

When $C_1/10$, ripple suppression is improved considerably with no fatal phase degradation. However, large C_2 values add excessive phase lag, increase oscillatory behavior, and reduce phase margin [17]. The extra pole helps to increase the order of phase accumulation, due to which the system is susceptible to variations in gain.

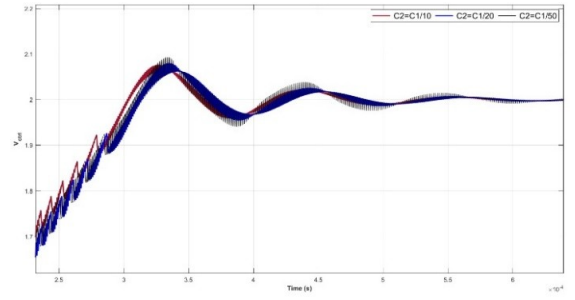


Fig. 6. Influence of C_2 ratio on third-order transient response.

As the C_2/C_1 ratio is increased, the added pole being inserted into the loop filter maps closer to the unity gain crossover region, resulting in an increased cumulative phase lag [26].

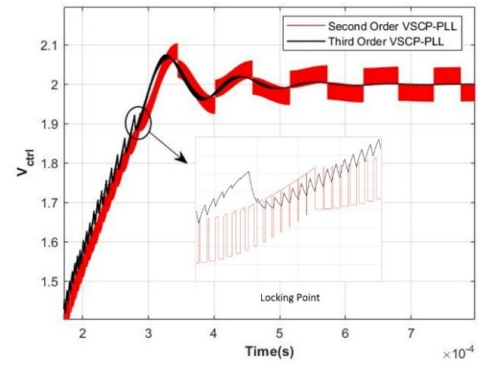


Fig. 7. Locking point phenomena of Second- and Third-order VSCP-PLL systems.

Fig. 7 further shows that the first jump in the second-order system is larger and oscillates around the locking point, indicating that the system takes longer to reach a steady state. In contrast, the third-order system shows a smaller initial jump with less oscillation, demonstrating better suppression of phase errors at the cost of a slower rise time [27]. The subsequent jumps in the second-order system appear as a series of oscillations, which eventually decay, but the system still exhibits some residual oscillation around the locking point.

4.3 Frequency-Domain Stability and Robustness Analysis

Time-domain transient responses give an intuitive insight into locking behavior, overshoot, and ripple behavior in Phase-Locked Loops (PLLs), but a thorough discussion of stability robustness needs to be conducted in the frequency domain [28]. The Bode plot provides one approach to the direct assessment of phase accumulation, gain crossover behavior, and sensitivity to loop gain perturbations that is of great importance for systems such as VSCP-PLLs.

The open-loop Bode plot of the second-order VSCP-PLL (Fig. 8) shows characteristics typical of a type-II second-order feedback system. The phase boost about the crossover frequency (6.15×10^4 rad/s) is relative to the dominant zero of the system, and the infinite gain margin (G_m) means that there is no threat of instability. The phase margin is 52.4 degrees; it helps in having a well-damped and stable system. This analysis is crucial

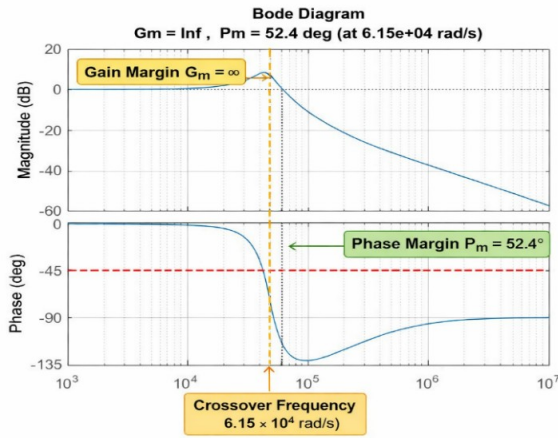


Fig. 8. Open-loop Bode plot of second-order VSCP-PLL.

in understanding the phase stability and robustness of the system to variations in the loop gain.

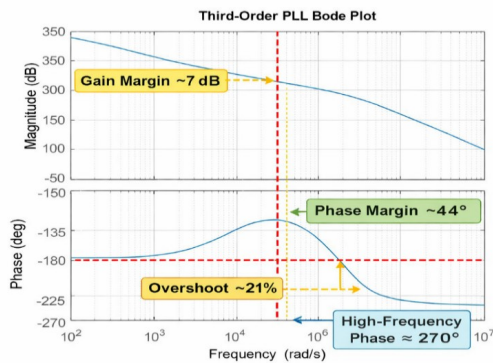


Fig. 9. Open-loop Bode plot of third-order VSCP-PLL.

The Third-order VSCP-PLL Bode plot, Fig. 9, gives important information about the stability properties of the system. The gain margin, or G_m , is about 7 dB (this means that the system has a moderate tolerance to increased open-loop gain before it becomes unstable). The phase margin (P_m) of 44° indicates that the system is well damped, which means that the system's response will be quite stable and there should be little danger of oscillations or instability. The plot also shows an overshoot of 21%, which indicates there is some deviation of the system from its steady-state value before it settles down, and is typical for a system having moderate damping. In addition, the high-frequency phase reaches about 270 degrees, which is the phase lag at a higher frequency and is characteristic of the behavior at those frequencies. Comparing the Bode plots of the second-order and third-order VSCP-PLLs shows a lot of differences in their stability characteristics [29, 30]. The 2nd-order system in Fig. 8 has an infinite gain margin and a 52.4° phase margin, meaning that the system has a higher tolerance to changes in loop gain and improved phase stability. However, the system has higher overshoot (approximately 12%) and a faster rise time for a faster but more oscillatory system response. In contrast, the third-order system (Fig. 9) has a moderate gain margin of about 7 dB, a slightly lower phase margin of 44° , and larger overshoot ($\sim 21\%$), indicating that there is a trade-off between stability and transient response. The third-order system, with its lower phase margin and greater overshoot, reveals that it is a little

less robust against gain perturbations, but it has better high-frequency attenuation with less suppression of reference spurs. Overall, the third-order system exhibits improved spectral purity and improved high-frequency performance, whereas the second-order system is more sensitive, with a minimum preparation time.

5. Conclusion

This work is a thorough analysis of the transient analysis and stability margins for second-order and third-order Voltage Switch Charge Pump Phase-Locked Loop (VSCP-PLL) architectures. By combining the methods of small-signal modeling and state-space modeling, Bode stability analysis, and nonlinear event-driven simulation, a unified model comparing the two loop orders under the same conditions was developed. The results show that loop order has a significant effect on the stability characteristics: the second-order design plan has predictable damping, infinite gain margin, ~ 52.4 -degree phase margin, and good gain-scaling robustness with $\sim 12\%$ overshoot. In contrast, the third-order loop provides improved high-frequency attenuation, meaning that 18 dB of reference spur suppression occurs at the expense of a reduced phase margin (~ 44 degrees) and increased overshoot ($\sim 21\%$), leading to sensitivity to gain variation. The analytical predictions agree well with nonlinear simulations (less than 3% deviation), emphasizing the fact that the trade-offs are structure-related, as opposed to being scales of parameters [17]. Overall, the work determines clear design guidelines: the second-order design is best for high lock times and low overshoot, while third-order design is best for high spectral purity and high ripple attenuation.

6. Future Recommendation

The Future Recommendations are:

Silicon Fabrication and experimental validation:

Design and implement the proposed 2.4 GHz Fractional-N VSCP-PLL in silicon and experimentally validate the lock-time, phase noise, and reference spurs, as well as its performance in realistic operating conditions such as supply voltage, substrate, and process variations.

Automated Design Optimization:

Embed the analytical stability constraints in a design approach that is driven by optimization for automatic sizing of the loop filter and charge pump using behavioral and event-driven models.

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Table 2

Summary of Simulation Results

Performance Metric	Second-Order VSCP-PLL	Third-Order VSCP-PLL
Loop Stability	Highly stable	Stable with reduced margin
Phase Margin	$\sim 52.4^\circ$	$\sim 44^\circ$
Gain Margin	Infinite	Lower than second-order
Overshoot	$\sim 12\%$	$\sim 21\%$
High-Frequency Attenuation	Moderate	Superior
Reference Spur Suppression	Moderate	~ 18 dB improvement
Gain Scaling Robustness	High	Moderate
Agreement with Nonlinear Simulation	$<3\%$ deviation	$<3\%$ deviation
Best Application	Fast locking and low overshoot	High spectral purity

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