

An improved fault current limiter for hybrid DC circuit breakers in large-scale MMC-HVDC systems

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KEYWORDS	ABSTRACT
Modular Multilevel-Converter HVDC System Protection Hybrid DC Circuit Breakers Fault Current Limiting Circuits	Designing multi-terminal HVDC systems presents significant challenges, particularly in control, modeling, and protection. One of the most critical concerns is the protection of these systems from DC short circuits. DC circuit breakers (DCCBs) have traditionally been a key solution for handling fault conditions. However, as these systems scale up to meet increasing power demands, the associated cost and technical complexity of deploying DCCBs across large-scale systems make them less practical and economically viable. This has driven the exploration of alternative or supplementary strategies to address short circuits more cost-effectively. In this regard, fault current limiter (FCL) circuits combined with DC breakers have been proposed to reduce their demands. This paper presents an improved non-superconducting FCL circuit paired with a hybrid DC circuit breaker to enhance system performance. The proposed topology integrates power electronic (PE) bidirectional switches, current-limiting inductors, and a discharging resistor. Simulations have been conducted using PSCAD/EMTDC software. An equivalent circuit model based on the Zhoushan HVDC project is used for simulation analysis to study behavior under the influence of this breaker. In contrast to current approaches that utilize continuous current-limiting components, the proposed topology minimizes power loss during normal operation. The simulation results show robust current-limiting performance, quicker fault isolation, and reduced energy absorption by the breaker. With the proposed circuit, the fault clearing time is improved by 23%, and energy absorption performance is enhanced by 98%. Compared to the existing topology in the literature the proposed design demonstrates superior current limiting performance. The proposed FCL reduces the fault current to 2 kA whereas the literature reported topology limits it to 2.5 kA. Further, it achieves significantly lower energy absorption, measured at 0.12 MJ compared to 0.4 MJ in the literature. A comparative analysis with the existing methods from the literature demonstrates that the proposed FCL offers superior current-limiting capabilities, faster fault response, and lower power losses.

1. Introduction

In modern electrical power systems, HVDC technology has become increasingly important because of its capacity to transmit electricity efficiently at longer distances and interconnect

asynchronous grids [1, 2]. Voltage Source Converter (VSC) based HVDC networks are especially preferred for their advanced capabilities such as bidirectional power flow, improved grid stability, and the integration of renewable energy sources [3]. However,

these systems are more prone to short-circuit faults which can disrupt operations and cause severe damage to equipment. Fault currents in HVDC systems pose a unique challenge compared to traditional AC systems due to the absence of a zero-crossing point in DC [4]. In VSC or modular-multilevel converter (MMC) based HVDC networks, a fault can result in rapid and high-magnitude current spikes, potentially exceeding the system's capacity to handle them [5]. Three types of DC breakers, including solid-state, mechanical, and hybrid breakers, have been employed to address the previously mentioned issues [6, 7]. Hybrid DCCBs have garnered significant interest from researchers and industries worldwide due to their important features, such as relatively low on-state losses, cost-efficiency, effective fault current handling, and suitable response times [8]. While these breakers offer essential capabilities for interrupting and clearing fault currents, they face challenges related to capacity limitations caused by high fault currents.

Additionally, the major drawbacks of DCCBs are the increased cost, size, and weight. Reducing the breaking current of these breakers can help lower their capital cost, size, and weight. Several approaches exist for handling the fault currents. These include reconfiguring the system, dividing the grid into separate sections, upgrading existing equipment, utilizing advanced control techniques, and integrating fault current limiters (FCLs) [9]. Among these, FCLs have demonstrated greater effectiveness in improving the reliability and stability of power grids [10]. FCLs are combined with DC breakers to limit high fault currents and protect HVDC lines from adverse effects [11]. While FCLs cannot completely isolate fault currents, they effectively suppress them. Modern FCLs keep their current-limiting components nonfunctional under normal situations, making them well-suited for systems with high power ratings [12]. An ideal FCL should exhibit low impedance in normal conditions and high impedance when a DC fault condition takes place. Further, it ensures that faults are rapidly limited, the system activates automatically and recovers quickly [13]. Additionally, it must be highly reliable in limiting fault currents without endangering operators, while also being compact, lightweight, and cost-effective to suit large-scale HVDC applications [14].

FCLs are generally categorized into three primary types: superconducting, non-superconducting, and hybrid technologies [13, 15]. The authors in [16] assess an innovative hybrid superconducting fault current limiting circuit that employs a biased magnetic field to limit fault currents. In [12], a novel hybrid FCL utilizing the push-pull method has been presented.

This design enhances current limiting performance by decreasing the rate of rise and the peak magnitude of fault currents. It improves current limiting capability by lowering the peak and rising rate of currents. In [17], a new FCL based on saturated core type, utilizing a permanent magnet and DC coil is proposed. The simulation results illustrate the FCL's efficiency in mitigating fault currents. Its efficiency is influenced by the value of the limiting reactor. In [18], FCL based on a current commutation is introduced. The limiter achieves substantial fault current reduction with minimal impact on the DC system by combining both half and full-control units. In [19], a current limiter circuit utilizing a liquid metal is suggested for medium voltage DC systems. Within 1.5 ms of activation, the fault current can be cut to half its value without the limiter. In [20] investigates three superconducting fault current limiters: the resistive SFCL, inductive shielded core SFCL, and saturated iron core SFCL. The study concludes that the saturated iron core-based SFCL performs best in HVDC networks and is likely to be used commercially. A novel self-adjusting fault current limiter (NSAFCL) topology has been proposed in [21]. In normal operation, the NSAFCL operates with parallel impedance. In fault mode, the impedance shifts to a series configuration, introducing a current-limiting resistor to reduce fault current and maintain fault voltage. In [22] a hybrid DC circuit breaker with current limiting capability is designed to limit fault currents and quickly isolate faults in the DC grid. This topology outlines the operation process, metal-oxide arrester (MOA) characteristics, and parameter design.

Additionally, a parallel energy dissipation circuit is incorporated to reduce energy dissipation in the MOA, shorten fault isolation time, and mitigate thermal effects on the MOA. A new fault current limiting circuit for the DC breaker was proposed in [23]. The design includes multiple units, categorized into two types: the main DC breaker and branch circuit breakers. In [11] the DC breaker with current limiting capability has been proposed. The circuit design features a current-limiting inductor connected in series with a switch. It offers effective current-limiting characteristics but requires multiple switches for handling large fault currents, which leads to substantial power loss during fault conditions. A hybrid breaker having self-adaptive fault current limiting feature was proposed in [24] and tested on a scaled-down circuit. It is observed that it successfully interrupts a 60 A fault current in 1.3 millis. However, multiple IGBTs increase system complexity, conduction losses, and costs. Moreover, reactors may experience saturation during fault current limitation,

allowing them to limit the surge of fault current but not its peak value.

Table 1

Literature of various proposed fault current limiting circuits

Reference	Method used	Advantages	Limitations
[11]	current limiting inductor in series with bidirectional switch	Efficient in handling the fault current and less energy is absorbed	Complex for large-scale systems due to multiple PE switches
[12]	The push-pull principle is used to limit the fault current.	Reduced rising rate and the peak of fault current	More complex
[16]	A biased magnetic field is used.	Effectively limit fault current.	Requires cooling system for superconducting material
[17]	DC coils and permanent magnets	Effective in fault current clipping	Focuses on particular design configuration
[18]	Uses current-commutation method	Effective in limiting the fault current	Complex control strategy
[19]	Uses liquid metal	Fast response due to fast switch and effectively limit fault currents.	Complex design due to the combination of fast switches and multiple CLIs
[20]	Resistive SFCL, inductive shielded core SFCL, and saturated iron core SFCL	Saturated iron core-based FCL outperforms in limiting the fault current	Requires expensive cooling system
[21]	Uses self-adjusting impedances	Effectively limit the fault currents without the need for	More losses due to utilization of current limiting components in

		external control	normal condition
[22]	Current limiting hybrid DC breaker	Effectively limits the rate of fault current increase	More losses
[23]	Uses additional breakers with the main breaker to limit the fault current	Effective in limiting the fault current	Complex design due to the use of additional breakers
[24]	Self-adaptive fault current limiting capability	Rapid fault isolation	Increased complexity due to a large number of IGBTs. Higher Conduction losses Higher overall system cost Tested for low power rating system
[25]	Uses flux-coupling FCL	Effective in decreasing the rising rate fault current	May pose significant losses due to the use of inductors in normal operation path

One of the challenges in previous designs of fault-current limiting breakers and FCLs is that the fault-current limiting components are active during normal operation which in turn poses unnecessary losses and leads to inefficiency. As the size of fault-current limiting components increases, larger components are needed, which worsens the situation further during regular operation. Some researchers have incorporated additional breakers to achieve current limiting characteristics for the main DCCB, but this significantly raises the cost of the protection system. Despite existing studies on DC breakers and FCLs, several issues remain unresolved, such as losses during the non-operational phase, current limiting capability, rapid fault isolation, size concerns, control challenges, coordination of control systems, and cost.

A recent study discussed in reference [25] explores three designs for magnetic flux-coupling solid-state fault current limiting circuits. These designs

incorporate mutual inductors and multiple power electronic switches. Using a comparison between current-limiting capabilities and structural complexities, the study identifies the flux-coupling DC limiter (FCDCL) as the most suitable option for installation in VSC DC grids. In normal operation, current flows through the limiting inductors which leads to increased power losses. The number of switches and MOAs in the proposed FCL design adds more complexity, which may hinder efficiency in real-world applications. This paper aims to address some of these issues and propose solutions. In this regard, this paper introduces an improved non-superconducting FCL topology for hybrid DC breakers designed to limit faults in MMC-based HVDC systems. A few of the concepts from reference [25] have been taken to reduce the fault current's rise rate and limit its magnitude, with modifications to address key issues and enhance overall performance. In [25], the limiting inductors remain part of the circuit during normal operation, which means that a larger inductor size can lead to significant power losses. However, the topology proposed in this paper eliminates the use of current-limiting components during normal operation which results in minimal on-state losses. It features a single semiconductor switch, two limiting inductors in parallel, and a discharging resistor. By utilizing parallel inductances, the fault current is evenly distributed across both branches and hence the current load on each inductor will be lowered. This design not only improves thermal management but also increases the FCL's overall reliability by mitigating the risk of overheating in any single inductor. Moreover, parallel inductances provide flexibility. If one inductor or branch fails, the other branch can still contribute to limiting the fault current. This setup enhances system reliability and ensures continuous fault current limiting functionality. However, in a series arrangement, the failure of even one inductor can result in the complete failure of the system. The resistor provides important benefits by dissipating the energy that is accumulated in the inductors. It effectively reduces the fault isolation time and minimizes the energy absorption of the breaker. Positioned within the fault path the resistor further limits the fault current hence the overall performance of the protection system will be enhanced. Fig. 1 presents the schematic diagram of the proposed FCL, while Fig. 2 illustrates the schematic of the FCL introduced in reference [25]. These FCL circuits are connected in series with the DC circuit breaker, with terminal A linked to the DC source and terminal B connected to the hybrid DC circuit breaker (HCB).

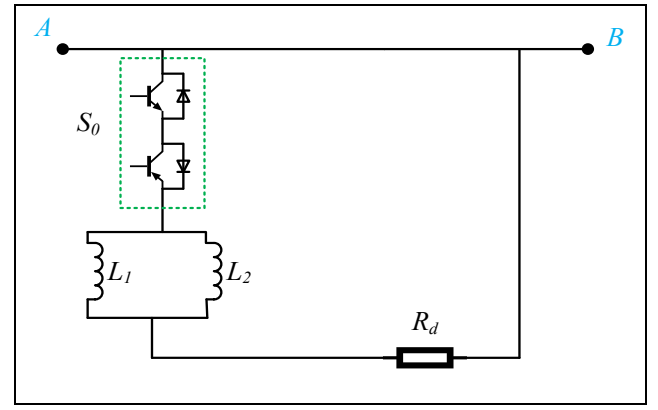


Fig. 1. Topology of proposed FCL

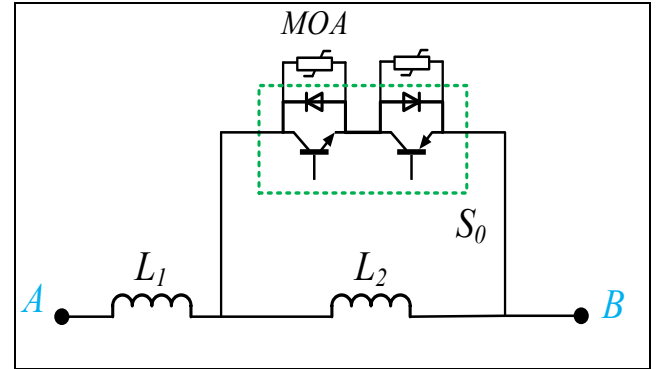


Fig. 2. Topology of the FCL circuit in [25]

This paper is organized in the following manner: Section 2 provides a methodology that includes an overview of the proposed FCL topology and the hybrid DC circuit breaker. It further explains an analysis of the operating principle of the proposed FCL and the method for selecting its key parameters. Simulation results and related discussion are presented in section 3. Section 4 summarizes the findings and offers the study's conclusions. Finally, future recommendations have been given in section 5.

2. Methodology

2.1 The proposed FCL topology and hybrid DC circuit breaker

This section describes the topology of the proposed FCL alongside the HCB developed by ABB. ABB's HCB is an advanced solution for protecting DC grids. It integrates fast mechanical switches with power electronics to enable rapid fault isolation and minimize energy dissipation. Fig. 3 shows a schematic representation of the ABB hybrid breaker. It is composed of three branches: the main current conduction branch which includes the mechanical ultra-fast disconnecter (UFD) and load commutation switch (LCS); the auxiliary branch also known as the current limiting branch; and the energy absorption branch which contains the MOA. Under normal operating conditions, current flows through the breaker's main branch. When a fault is detected, the LCS in the main branch opens, redirecting the current to the auxiliary branch, which is limited based on

design specifications. Following this, the remaining current is directed to the arrester branch, effectively isolating the fault current and protecting the system. It achieves ultra-fast current interruption and reduces system stress during fault events.

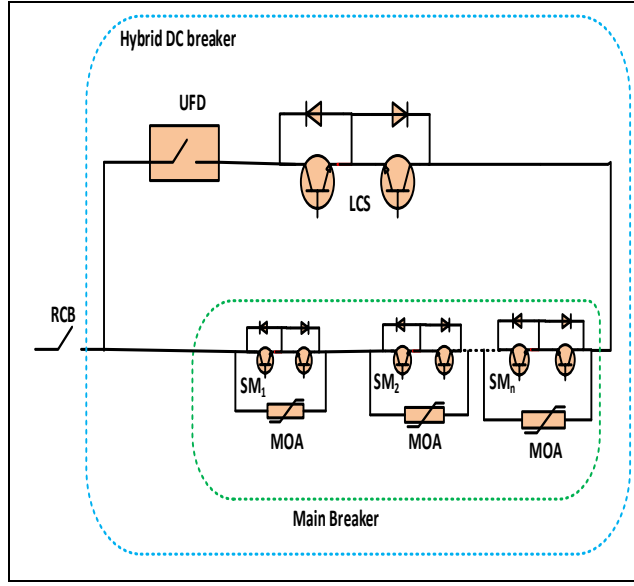


Fig. 3. ABB's hybrid DC breaker [26]

The proposed FCL significantly improves the breaker's performance by limiting the fault current before it reaches critical levels. The proposed topology not only reduces the rate of fault current rise but also enhances overall system protection, improves grid stability, and minimizes system downtime. The FCL design includes a single bidirectional switch in the main path, along with two inductors, L_1 and L_2 , which act as the primary current-limiting components during fault conditions. The design also incorporates a resistor (R_d) which helps further limit the fault current, reduce energy absorption across the breaker, and shorten fault isolation time. The complete schematic of the proposed FCL and HCB is illustrated in Fig. 4.

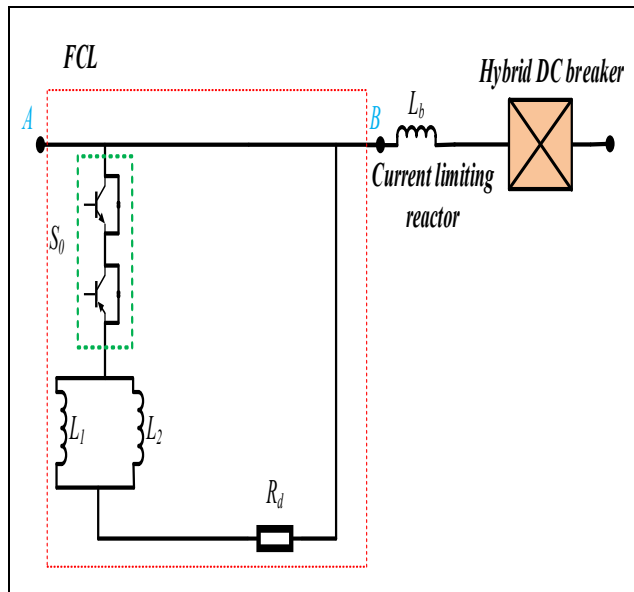


Fig. 4. Complete schematic of FCL and hybrid DC breaker

2.2 The operational principle of the proposed FCL circuit

The proposed scheme is divided into four operating phases to clarify its functionality. Fig. 5 illustrates the different operational stages over time and the overall behavior of the DC when FCL is used. In the time interval from 0 to t_1 , normal current flows in the system and follows a normal path in FCL and the breaker's main branch. In Fig. 6(a), the red dotted line indicates the current flow during this period. The current in the normal stage refers to the system's rated current, which is determined by the design specifications. At t_1 , a potential fault is identified in the network. Once identified, confirmation generally requires a few millis. During this period, current keeps flowing through the breaker's main branch while the switches begin opening progressively. During this time, the flow of current remains in the same direction as in the 0 to t_1 period as illustrated in Fig. 6(b).

Upon fault confirmation at t_2 , the main branch switches open, redirecting the fault current to the current-limiting components in the FCL and auxiliary branch of the breaker. At this point, the process of fault current limitation is activated. Fig. 6(c) shows the flow of current during the t_2 to t_3 interval. After t_3 , the auxiliary branch switches open in the breaker, directing the remaining fault current to the arrester. The current-limiting branch after t_3 is detached from the circuit. This is achieved by opening the switches in the auxiliary branch, which redirects the remaining fault current to the arrester branch for energy dissipation. The FCL's current-limiting components (inductors L_1 and L_2 , and resistor R_d) are no longer active in the circuit after this stage. At this period, the fault current is brought to zero and fully isolated.

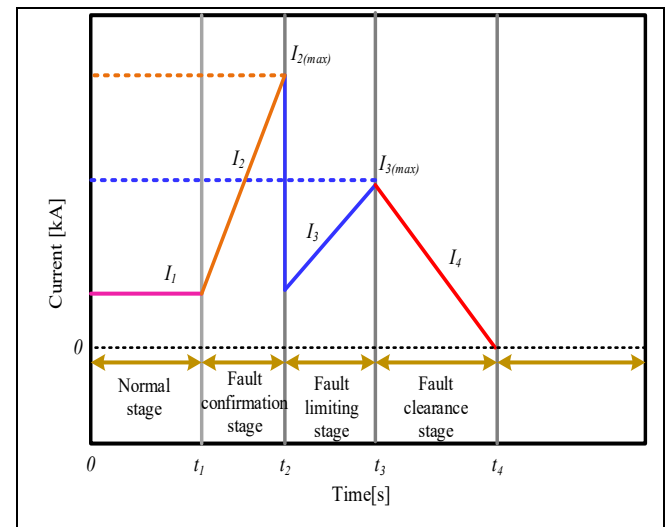


Fig. 5. The overall behavior of DC under the impact of FCL circuit with different operating periods

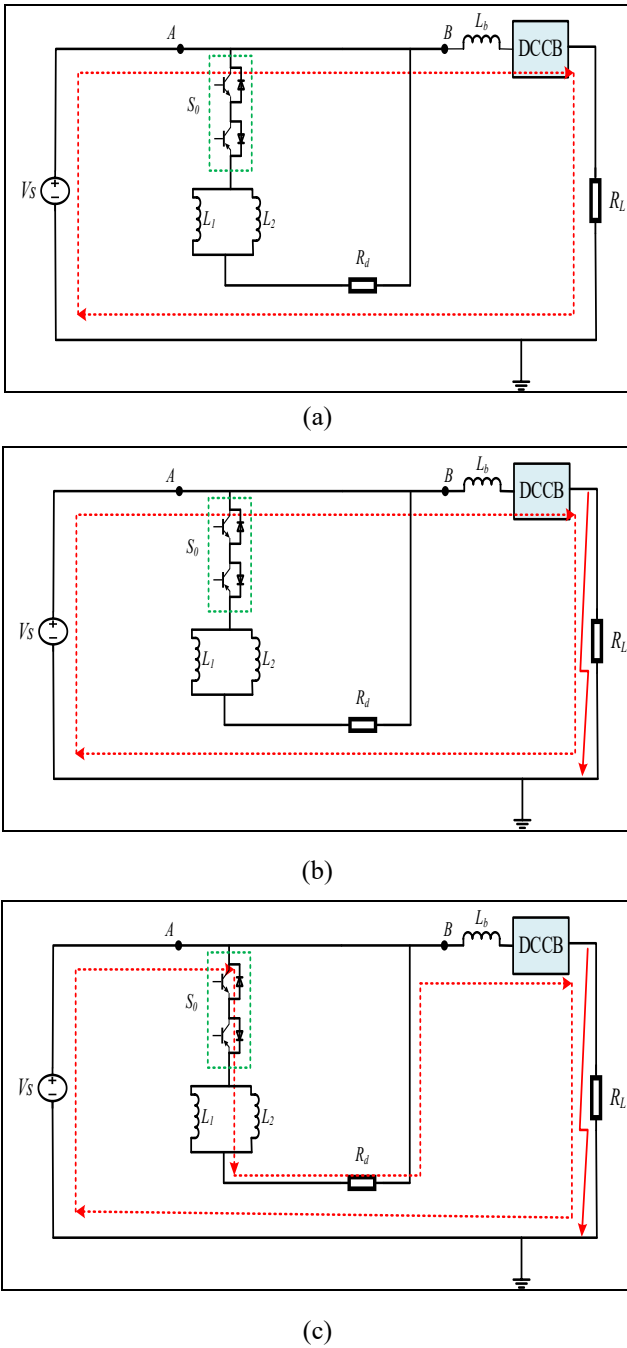


Fig. 6. Equivalent circuit during different operations (a) normal operation stage (b) current raising/confirmation stage (c) current limiting stage

2.3 Selection of parameters for proposed FCL circuit

To select the appropriate inductance for the main breaker branch (L_b) and the current limiting inductors (CLIs) in the proposed FCL, it is necessary to calculate the current at different stages. The equivalent circuit for calculating the current limiting reactor (L_b) and CLI values is split into two parts: the system's equivalent circuit before the fault and following the fault. Fig. 7(a) depicts the equivalent circuit for the periods 0 to t_1 and 7(b) depicts the equivalent circuit for the periods t_1 to t_2 . The internal resistance of the switches is negligible and has accordingly been excluded for simplicity. Fig. 7(c) shows the third equivalent circuit representing the fault current limiting stage during the interval t_2 to t_3 .

In designing the various components of the FCL circuit and the L_b of the breaker, the following key considerations must be kept in focus.

- The peak line current should remain below the maximum interruption capacity of the DC breaker.
- The line current's rate of increase should not exceed the maximum permissible change rate for the breaker's current.
- The fault current needs to be isolated prior to the DC link capacitors are fully discharged.

Mathematically, the above points can be expressed as:

$$\llbracket i_{line} \rrbracket^{max} < i_{DCCB}^{max} \quad (1)$$

$$\left(\frac{di_{line}}{dt} \right)^{max} < \left(\frac{di_{DCCB}}{dt} \right)^{max} \quad (2)$$

$$t_{fc} < t_{cd} \quad (3)$$

In equation (1) $\llbracket i_{line} \rrbracket^{max}$ represents the maximum value the system can reach when a fault occurs and $\llbracket i_{DCCB} \rrbracket^{max}$ indicates the maximum current value that the DCCB can withstand and interrupt. From equation (3) t_{fc} indicates the overall time required to clear the fault and t_{cd} represents the time needed to discharge the DC-link capacitors.

In the interval from 0 to t_1 , the current rises from zero value to the rated one predefined as the system line current. This current is given by equation (1), where I_s represents the rated line current.

$$I_s = I_1 \quad (4)$$

When the fault is detected at t_2 , it requires a few moments to confirm its presence. Throughout this period, the flow of current will be through the breaker's main branch, and the voltage and current expressions during this time can be determined through the equivalent circuit illustrated in Fig. 7(b) [27, 28].

$$u(t) = \frac{V_1 \omega_0}{\omega_n} e^{-\gamma(t-t_1)} (\sin(\omega_n(t-t_1)) + \xi) - \frac{I_1}{C \omega_n} e^{-\gamma(t-t_1)} \sin(\omega_n(t-t_1)) \quad (5)$$

$$I_2(t) = -\frac{I_1 \omega_0}{\omega_n} e^{-\gamma(t-t_1)} (\sin(\omega_n(t-t_1)) - \xi) + \frac{V_1}{\omega_n(L_b + L_{line})} e^{-\gamma(t-t_1)} \sin(\omega_n(t-t_1)) \quad (6)$$

Whereas, the co-efficient presented in Equation (5) and Equation (6) are detailed as:

$$\omega_0 = \sqrt{\gamma^2 + \omega_n^2} \quad ,$$

$$\omega_n = \sqrt{1/(L_b + L_{line})C + \gamma^2} \quad ,$$

$$\gamma = (R_{line}/2(L_b + L_{line}))$$

and

$$\xi = \arctan\left(\frac{\omega_n}{\gamma}\right)$$

The estimation for the L_b of the main branch using equations (5) and (6) is complex. Since the voltage fluctuations caused by the DC-link capacitors are negligible, they can be treated as a DC source to simplify the calculations mathematically. With this supposition, KVL and the Laplace transformation are reapplied to the equivalent circuit depicted in fig. 7(b). The resulting expression is provided in equation (7) for the short interval t_1 to t_2 .

$$I_2 = \frac{V_1}{R_{line}} - \left(\frac{V_1}{R_{line}} - I_1\right)e^{-\alpha(t-t_1)} \quad (7)$$

Where, $\alpha = R_{line}/(L_b + L_{line})$

In equation (7), I_2 is the maximum allowable range of fault current that the breaker can safely handle.

V_1 is the rated voltage, R_{line} is the resistance and L_{line} is the inductance of the line. I_1 is the rated current, and these depend on the system's initial conditions.

By considering two key factors, the maximum allowable fault current range and the time required to reach it, a realistically correct value for the breaker inductance L_b can be approximated.

Using equations (7), and (1) (2) and (3), a MATLAB program was developed to simulate the impact of fault current by testing different inductance values and varying fault locations relative to the reference HVDC terminal. Fig. 8 illustrates the effect of L_b on I_2 , showing that as L_b increases, the values of I_2 decrease by the end of the fault-current confirmation stage. Additionally, it highlights that fault occurring closer to the set point terminal have a more noticeable impact. If the fault current's rate of increase is set at 3.5 kA/ms as noted in [26] and the fault is located 100 km from the terminal T-I, then, based on equation (7) and constraints in equations (1) (2) and (3), L_b can be estimated to 37.5 mH, with I_2 reaching a maximum of 7.5 kA during a fault-confirmation interval of 2 ms

At time t_2 the fault is confirmed. Immediately afterward, the fault current limitation process begins. Here, the total inductance of the current limiting inductors is considered as L_{eq} to avoid mathematical complexity. In this stage, diagram of the equivalent circuit is illustrated in Fig. 7(c). Applying KVL to the circuit depicted in Fig. 7(c) leads to the following mathematical equation.

$$I_3 = \frac{V_1}{R_{line}+R_d} - \left(\frac{V_1}{R_{line}+R_d} - I_2\right)e^{-\beta(t-t_2)} \quad (8)$$

β coefficient is used in equation (8) and can be defined as: $\beta = R_{line}+R_d/L_{eq} + L_b + L_{line}$

The variables associated with Equation (8) are explained as: I_3 is the reduced fault current achieved after the fault-current limiting process; I_2 is determined by the initial conditions and can be determined by Equation (7). L_{eq} and R_d show the equivalent current-limiting inductor and the discharging resistor used in the FCL, respectively. The component sizes in the FCL can be determined using Equation (8). The system handles the current I_3 during the interval t_2 to t_3 . Using Equation (8), computational algorithms in MATLAB can be used to analyze the relationship amongst I_3 , L_{eq} , and R_d .

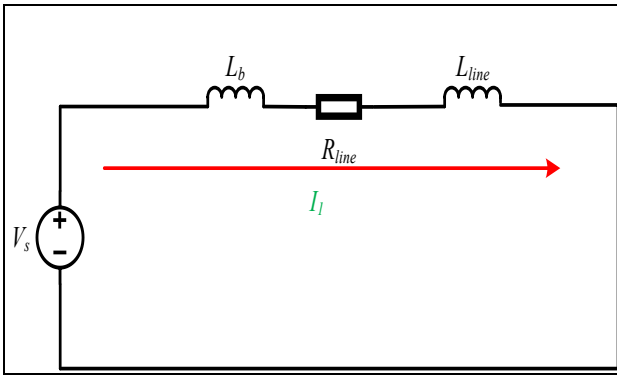
Fig. 9 illustrates the relationship among I_3 , L_{eq} , and R_d , with the fault location set at 100 km from terminal-1, and the durations for the fault-current limitation stage set to 2.5, 3, 3.5 4, and 4.5 millis. The results shown in Fig. 9(a) and 9(b) indicate that increasing L_{eq} , R_d , and the duration of the fault-current limitation stage results in a decrease in fault current to its least achievable values. Subject to the constraints outlined in equations (1) (2) and (3), and the calculations in equation (8), appropriate values for L_{eq} and R_d can be estimated. For this work, a 3 ms duration is chosen for the fault current limiting stage, and corresponding values for L_{eq} and R_d are determined correspondingly.

Subsequent to t_3 the remaining fault current is directed to the arrestor branch, where the remaining power is dissipated during this final stage. Therefore, the energy absorbed by the arrestor can be determined with equation (9). At this stage, the mechanical switch is then opened to isolate the faulty section of the line. In equation (9), E denotes the energy, while $I(t)$ and $V(t)$ refer to the instantaneous current and voltage across the arrestor, respectively.

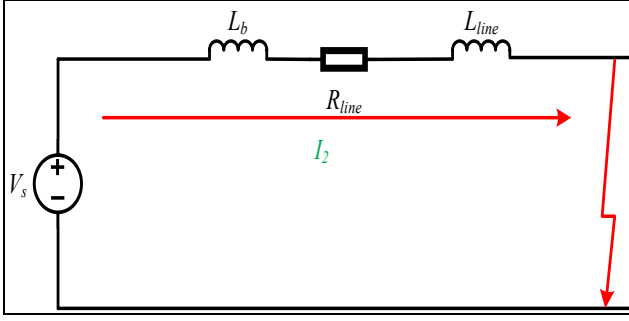
$$E = \int V_{MOA}(t)I_{MOA}(t)dt \quad (9)$$

3. Results and Discussion

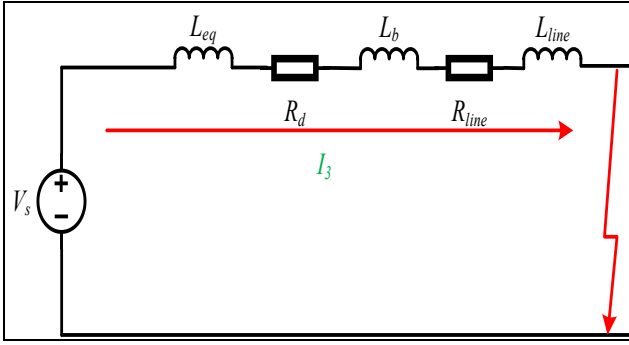
The effectiveness of the proposed FCL circuit is assessed through simulations conducted in PSCAD/EMTDC, with the results analyzed accordingly. This study uses an equivalent circuit modeling method of Zhoushan MMC-based HVDC grid for the simulation analysis. The parameters for the equivalent circuit are provided in Table 2 and the FCL parameters are provided in Table 3.



(a)



(b)



(c)

Fig. 7. Simplified equivalent circuits (a) normal operation stage (b) current Raising/confirmation stage (c) current limitation stage

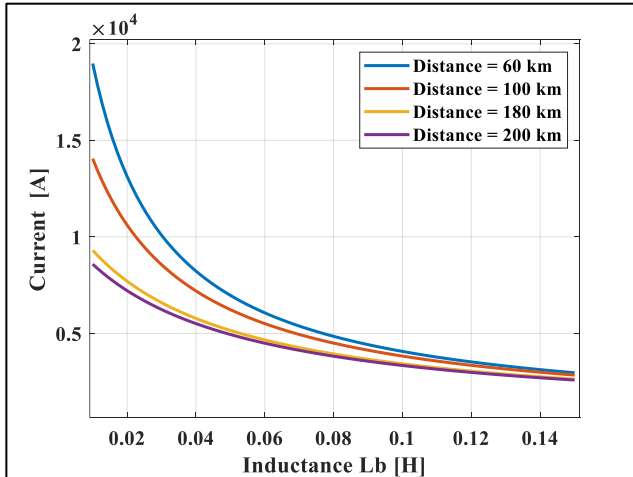
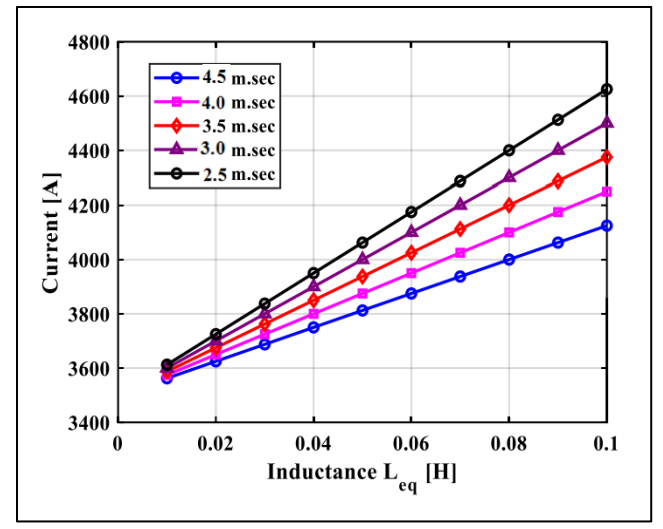
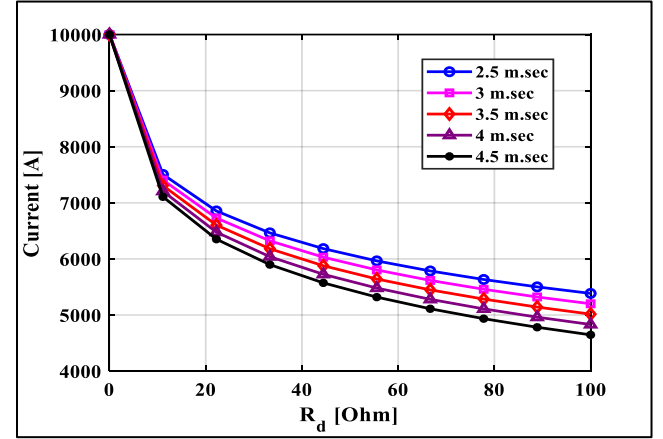


Fig. 8. Effect of breaker impedance variations on current



(a)



(b)

Fig. 9. (a) Effect of L_{eq} on I_3 (b) Effect of R_d on I_3

Table 2

Considered equivalent circuit parameters for Zhoushan DC grid

Parameter	Value
Considered Terminal Voltage	± 200 kV
Line Current	0.5 kA
Cable length	200 km
Location of fault	100 km (Terminal-I)
Line Resistance/km	0.035 ohm/km
Inductance/km	0.156 mH/km

Table 3

Proposed FCL parameters

Parameter	Value
Current limiting Reactor	L_b 37.5 mH
Equivalent Inductance	L_{eq} 100 mH
Discharging Resistor	R_d 50 ohms

The Zhoushan Archipelago, part of China's eastern coastal region, is situated among thousands of islands.

The Zhoushan HVDC grid, located in China's Zhejiang province, is an important multi-terminal HVDC project designed to improve power transmission efficiency and reliability in the region. The project details are briefly outlined in studies by [29] and [30], while [31] discusses more recent upgrades to the system. The Zhoushan HVDC grid consists of five terminals using cutting-edge MMC technology. It connects several islands, including Zhoushan Island, with the mainland grid, addressing the challenges of renewable energy integration and long-distance power transmission. The DC voltage rating for the converter valves is ± 200 kV. The project has a total power capacity of 1000 MW and a total cable length span of 141.5 kilometers. This project has a significant impact on supporting the region's economic development and renewable energy goals by providing a robust and efficient power transmission infrastructure. The schematic of Zhoushan HVDC grid is shown in Fig. 10.

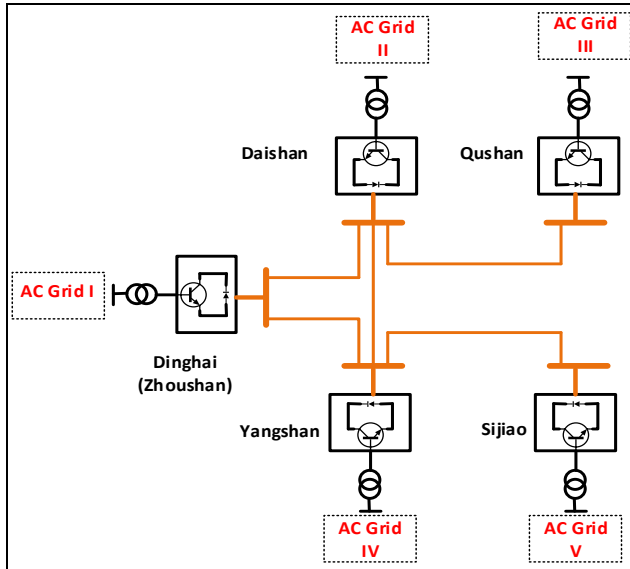


Fig. 10. Schematic diagram of the Zhoushan HVDC grid

For the analysis, the block diagram in Fig. 11 illustrates the placement of breakers, and the FCLs between terminals: Terminal T-1 and Terminal T-2. A line-to-line fault (L-L) is introduced on the transmission line at a designated distance from T-1. The simulation results are grouped into two sections. The first section presents the results for a conventional HCB without FCL and with FCL and their comparison. The second section compares the results of three scenarios: the system without a FCL, the proposed FCL, and the FCL discussed in the literature. This section provides a detailed comparative analysis of these configurations, highlighting the performance improvements and limitations of each approach. These results pertain to the DC voltage, current, and power absorbed by the MOA inside the hybrid DC breaker. Fig. 12 illustrates the voltage and current profiles of the system during an L-L fault condition. According to

the parameters outlined in Table 2, the simulation results for current and voltage are depicted in fig. 12(a) and 12(b) respectively. Initially, from 0 to 0.3 s, the system functions under standard operating conditions, with a current of 0.5 kA and a voltage of ± 200 kV which are the rated values of the system. At 0.3 s, the fault occurs in the system and causes the current to rise rapidly. Simultaneously, the DC capacitors begin to discharge. When capacitors are fully discharged, the voltage and current decrease to zero.

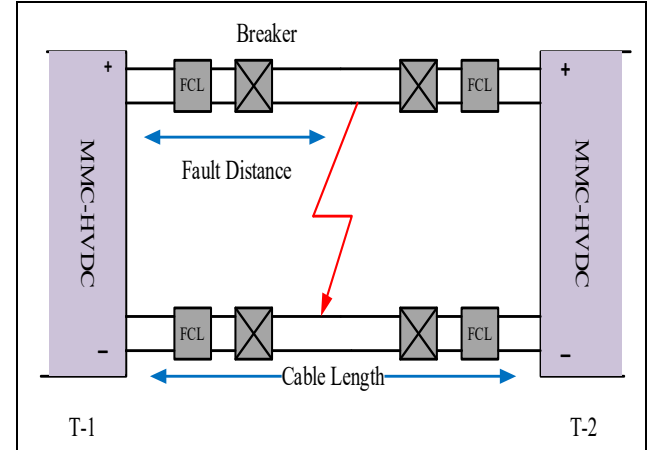
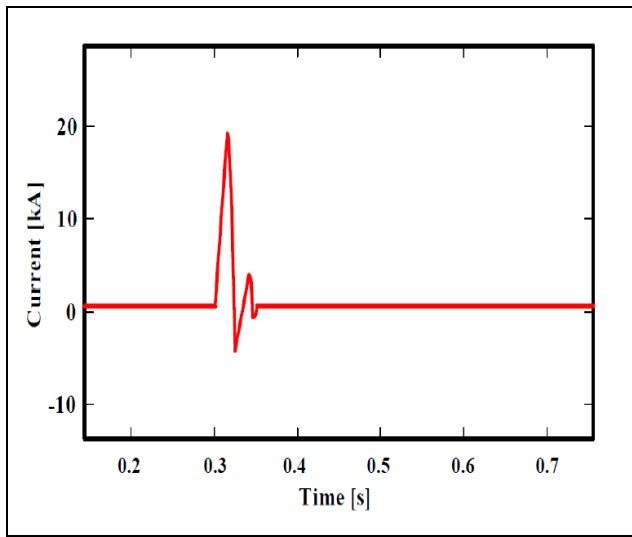


Fig. 11. A Block diagram illustrating the simulation design

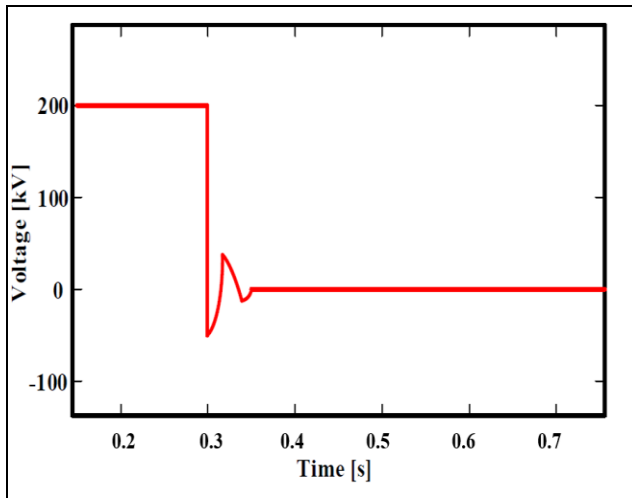
3.1 Primary results with non-FCL and FCL circuit

Fig. 13 illustrates the response of the overall fault current over time, comparing the results with and without the FCL. Following the fault injection at 0.3 s, the current rapidly escalates, reaching about 7.5 kA by 0.302 s. It continues to surge sharply and touches the peak at nearly 16 kA by 0.304 s. This shows a significant rise in fault current without any limiting component, reflecting the high fault current in the system. With FCL, when a fault is introduced at 0.3 s, the current rises similarly at first and reaches almost 7.5 kA. At 0.302 s, the FCL starts to operate and limits the current. The fault current is significantly reduced with a steep drop occurring after 0.302 s. It remains much lower and prevents the sharp rise observed in the absence of the FCL. By 0.304 s the current stabilizes at a very low value of around 2 kA. This demonstrates the FCL's effectiveness in mitigating the fault current. The results present that the peak fault current is reduced by up to 51.25%, and the proposed FCL enhances fault isolation time by up to 23.64%.

The supplementary results provide insights into the current flow through the main, current limiting, and energy absorption branches of the breaker with FCL, as illustrated in Fig. 14(a), (b), and (c) respectively. These findings capture the behavior of the DC at various durations. Fig. 14(a) represents the current through the LCS, illustrating that from 0 to 0.302 s, the current follows the path of main branch. At 0.302 s, the switches get fully opened, bringing the current to



(a)



(b)

Fig. 12. Current and voltage profile of the system during L-L fault (a) current (b) voltage

zero. Similarly, Fig. 14(b) illustrates that the FCL circuit remains deactivated until 0.302 s, after which the fault current limiting function engages, limiting the current in this branch to approximately 2 kA due to the current-limiting components. At 0.305 s the switches in the FCL open causing the current in this branch to drop to zero. Immediately after 0.305 s, the remaining current commutates to the arrestor branch as depicted in Fig. 14(c).

Fig. 15 depicts the voltage behavior across the breaker. The FCL significantly lowers the peak voltage from approximately 700 kV (without FCL) to around 400 kV (with FCL). The voltage with the FCL is more stable and avoids extreme spikes observed without it. This result clearly shows the effectiveness of the FCL in mitigating voltage spikes and enhancing system reliability during fault conditions.

Fig. 16 highlights the essential function of the FCL in reducing the energy absorbed by the MOA, thereby alleviating stress on the system and ensuring more effective fault management. The FCL significantly

reduces the energy absorbed by the MOA decreasing it by approximately 98.67%, from 9 MJ without the FCL to only 0.12 MJ with the FCL. By incorporating the FCL, the energy load on the arrestor is minimized which prevents potential overload and enhances system reliability during fault conditions.

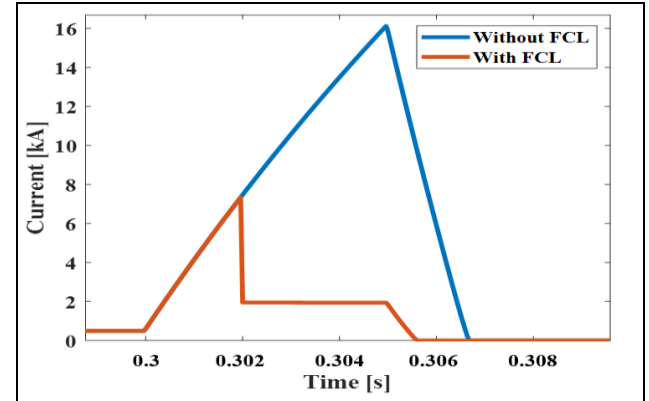


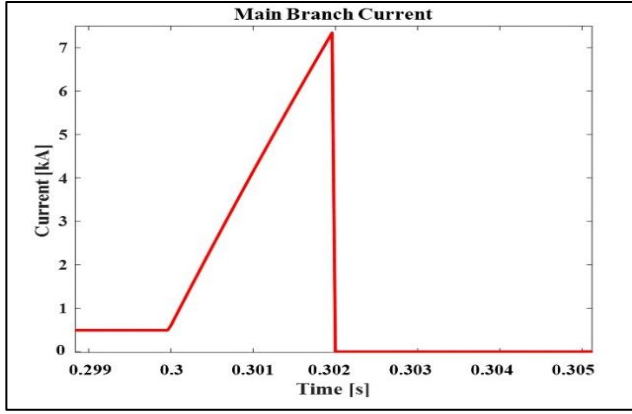
Fig. 13. Fault current with FCL

3.2 Comparative analysis of non-FCL, FCL1 [32], and proposed FCL

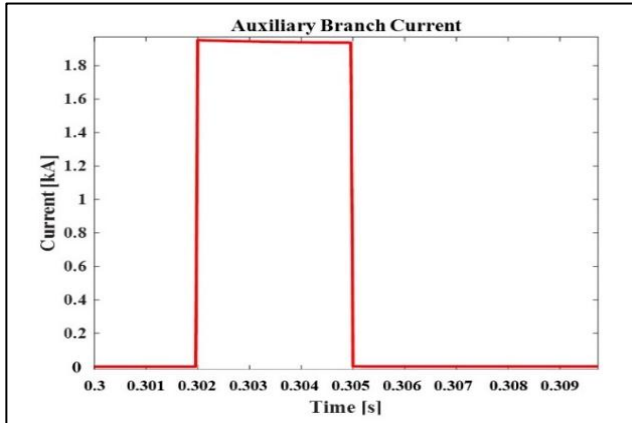
This section compares the results of the proposed FCL topology with those of the non-FCL and FCL topology presented in [32]. For clarity, the FCL topology from [32] will be referred to as FCL1. The performance analysis between the proposed topology and FCL1 will highlight the improvements and distinctions. A detailed comparison is conducted concerning operational efficiency, fault current limiting capabilities, energy absorption, and voltage drop across the breaker. Through this, a clearer understanding of the advantages offered by the proposed topology is provided. The results are critically examined to assess their practical implications. Further, Table 4 has also been provided for comparing the proposed design with [24] and [32] topologies in the literature.

A comparison of fault current behavior among non-FCL, FCL1 (blue dotted line), and the proposed FCL (solid green line) is illustrated in Fig. 17. Focusing on FCL1 and proposed FCL, it is observed that both FCLs initially follow the same current path, with the fault current rising rapidly after 0.3 s and peaking at approximately 7.5 kA around 0.302 s. However, the proposed FCL shows a more effective current-limiting performance, reducing the fault current more sharply and stabilizing it close to 2 kA after 0.304 s. In contrast, FCL1 exhibits a slower decline in current, maintaining a higher current level for a longer duration before reducing to the same level as the proposed FCL. This demonstrates that the proposed FCL provides

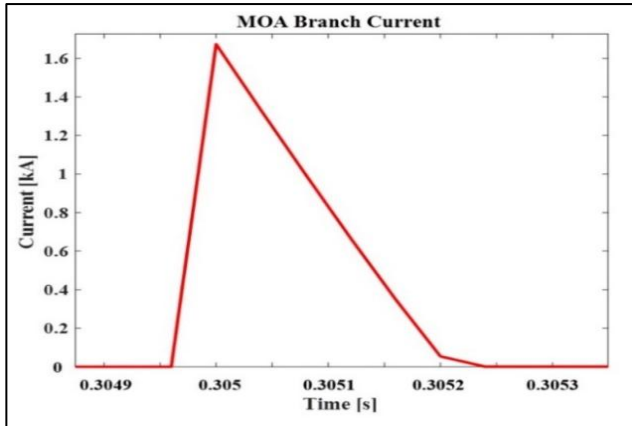
faster and more efficient fault current suppression than the FCL1.



(a)



(b)



(c)

Fig. 14. Current response in different branches of HCB (a) main branch current (b) auxiliary branch current (c) arrester branch current

Fig. 18 compares the voltage across the breaker. In simulation results, FCL1 and the proposed FCL-based system experience a voltage spike after 0.302 s due to the fault. However, FCL1 exhibits two sharp voltage peaks, reaching nearly 650 kV and 600 kV, indicating significant stress on switches. These spikes occur at around 0.302 s and again after 0.304 s, showing more stress when used in large-scale HVDC systems. In contrast, the proposed FCL effectively limits the

voltage spike to about 400 kV and provides a much smoother transition, gradually returning to a stable voltage level by 0.305 s. This demonstrates that the proposed FCL offers better voltage control and reduces the magnitude of voltage spikes.

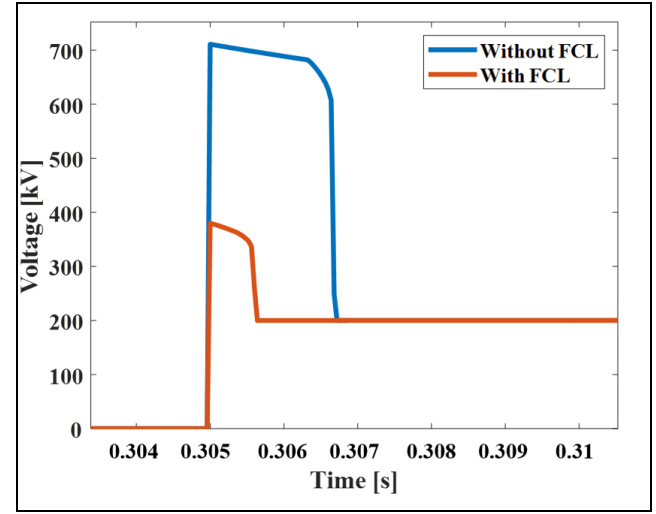


Fig. 15. Voltage behavior across breaker with FCL

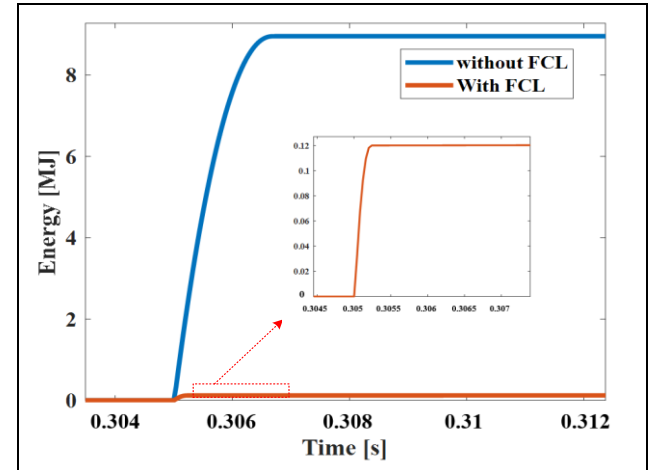


Fig. 16. Energy absorbed by MOA

Fig. 19 depicts the energy absorption results during fault conditions. FCL1 absorbs a significantly higher amount of energy, reaching around 0.4 MJ shortly after 0.305 s. In contrast, the proposed one absorbs considerably less energy, measured at approximately 0.12 MJ. This indicates that the proposed FCL is much more efficient in limiting energy absorption during fault events, which reduces stress on the system and enhances its overall performance and durability compared to FCL1.

4. Conclusion

This paper presents an improved FCL topology that consists of a bidirectional power PE switch, current-limiting inductors, and a discharging resistor. During normal operation, the absence of current limiting components in the main current path ensures

negligible power losses. In the event of a fault, these components are activated and effectively limit the fault current to 2 kA. The discharging resistor facilitates the release of stored energy from the inductors. This feature reduces energy absorption from 9 MJ to 0.12 MJ and improves the breaker's fault isolation time by 23%. The proposed design's

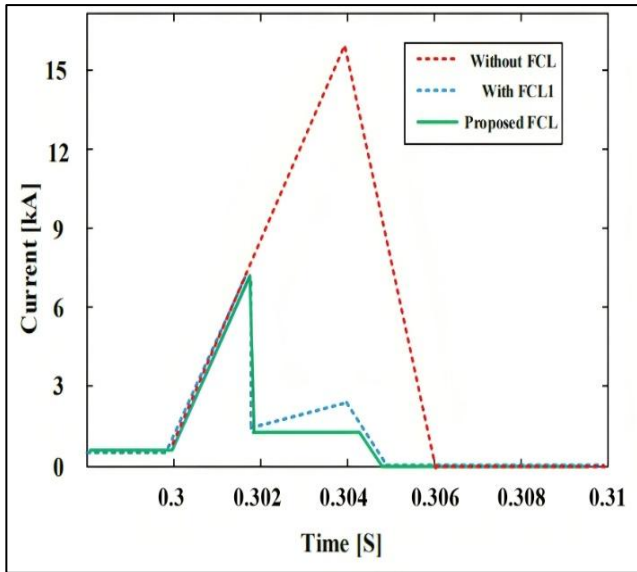


Fig. 17. Response of fault current

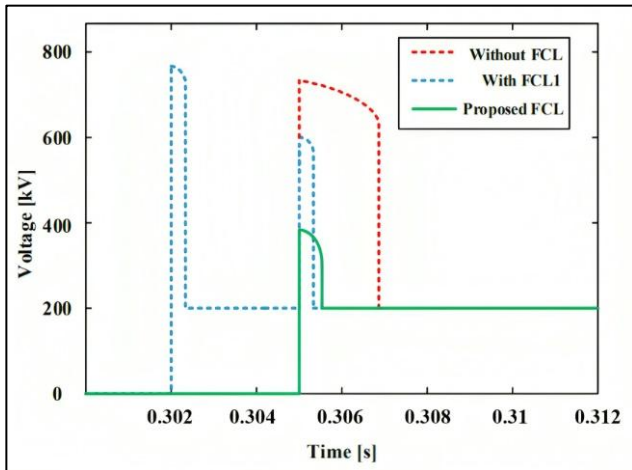


Fig. 18. Voltage behavior across the breaker

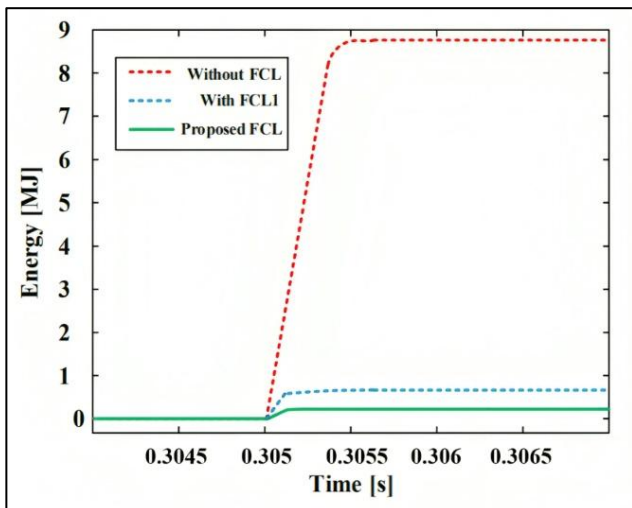


Fig. 19. Energy absorbed by the MOA

Table 4

Performance comparison of the proposed FCL against other topologies in the literature

Scheme	Reduction in peak fault current (%)	Voltage stress	Power losses
[32]	53	Higher	High due to the insertion of PE switches
[24]	28.5	Higher	Higher owing to addition of PE switches in limiting path
Proposed	53	lower	Lower due to the absence of PE switches in normal operation

effectiveness has been validated through PSCAD/EMTDC simulations. The results show excellent current limiting performance, minimal power losses in the on-state, and greatly reduced energy absorption. Comparative analysis with one of the existing topologies in the literature confirms the advantages of the proposed FCL, as it limits fault current to 2 kA whereas, the design in the literature limits it to 2.5 kA. Additionally, the proposed topology achieves energy absorption of 0.12 MJ, a considerable enhancement over the 0.4 MJ observed in the previous design. The voltage stress across the breaker is lower compared to existing topologies. Due to this, the strain on switching components will be reduced. These findings highlight the proposed FCL as a promising solution for effective fault current limitation and isolation in large-scale MMC-based HVDC systems.

5. Future Recommendations

Future research on FCL with hybrid DC breakers should focus on optimizing control strategies through AI-based models and real-time fault prediction models. Further research is needed to improve energy efficiency with advanced materials and ensure scalability for large-scale power systems. For practical deployment, experimental validation through hardware implementation is essential for real-world applicability. Furthermore, resilience to high-frequency transients and electromagnetic interference should be examined to improve robustness. Given the increasing integration of renewable energy, future studies should explore its application in micro grids and offshore wind farms to improve fault protection and overall system reliability. Finally, a comprehensive economic and environmental impact

assessment should be conducted to assess the feasibility of integrating these technologies into future RE systems.

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